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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/719,192	BAEK ET AL.	
	Examiner	Art Unit	
	Leila Malek	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12* is/are allowed.

6)☒ Claim(s) *1-7 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 11/14/2007 have been fully considered but they are not persuasive.

Applicant's Argument: Applicant argues, on page 10, that Busching is not directed to an OFDM receiver.

Examiner's Response: In response to applicant's arguments, the recitation "OFDM signal" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Applicant's Argument: Applicant argues, on page 10, that Busching does not teach or suggest a frequency domain equalizer as recited in claim 1.

Examiner's Response: Examiner asserts that Busching does not expressly discloses that the equalizer is a frequency domain equalizer, however in column 12, lines 65-67, Busching discloses that the equalizer 51 is employed to equalized the frequency response of the transmission channel in the region of the transmission bandwidth form. Therefore equalizer 51 is a frequency domain equalizer.

Applicant's Argument: Applicant argues, on page 10, that Busching does not teach or suggest that an FFT processing is performed during the demodulation.

Examiner's Response: Examiner asserts that Busching discloses that the pulse response and the coefficient set for the equalizer filter 51 are calculated with the aid of an FFT (see column 11, lines 40-44). Therefore an FFT processing is performed during the demodulation.

Applicant's Argument: Applicant argues, on page 11, that Busching does not teach or suggest that the output of the FFT processing is a transformed preamble that is either stored, output, or synchronized with a clock frequency of the FFT processor.

Examiner's Response: Examiner asserts that Busching does not expressly disclose that the equalizer synchronizes the output of the signal converter with a clock frequency of the fast Fourier transform processor, and outputs a synchronized second long preamble and second data. However it would have been obvious to one of ordinary skill in the art at the time of invention to synchronize the output of the signal converter with a clock frequency of the FFT to synchronously process the data and the preamble and therefore prevent having overflows of data.

Applicant's Argument: Applicant argues, on page 11, "the office action asserts that "it would have been obvious to one of ordinary skill in the art at the time of invention to synchronize the output of the signal converter with a clock frequency of the FFT to synchronously process the data and preamble and therefore

prevent having overflows of data.". However, this assertion overlooks the fact that the data signal of Busching is not processed with an FFT processor."

Examiner's Response: Examiner asserts that, Busching in column 6, lines 25-26, discloses that the received signal (i.e. the data signal and the preamble) is supplied to a functional block 44 whose object is to recognize and analyze the received signal. Busching further discloses that equalizer 51 is employed to equalize the frequency response of the transmission channel in the region of the transmission bandwidth form (see column 12, lines 65-67). Therefore since the equalizer is a frequency-domain equalizer, preamble and the data signal both need to be transformed to the frequency domain and therefore need to be processed by the FFT processor.

Applicant's Argument: Applicant argues, on pages 11 and 12, "a skilled in the art would not modify a non-OFDM system such as Busching to use the synchronization techniques of Schmidl".

Examiner's Response: Examiner asserts that the motivation used to show the obviousness of combination of the two references is not relevant to the fact that the first reference is a non OFDM system. The motivation cited by the examiner shows an advantage that the system disclosed by Schmidl can provide a system like the one disclosed by Busching.

Applicant's Argument: Applicant argues, on page 13, that "The office action does not indicate how the cited references teach of suggest a buffer and the first data directly input to the frequency converter into second data in the frequency domain.".

Examiner's Response: Examiner asserts that Schmidl further shows (see Fig. 5) a Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble (i.e. the training symbol) and first data, the FFT processor comprising: an input buffer that is configured to temporarily store the first data (122 in figure 5); a memory that is configured to store the first long preamble (122 in figure 5, note that the symbol include data and training symbol (i.e. preamble), page 16, lines 3-36); and an FFT unit that is configured to transform the first long preamble in the memory into a second long preamble in a frequency domain and to store the second long preamble back into the memory, to transform the first data that is temporarily stored in the input buffer and the first data directly input to the frequency converter (as shown in Fig. 5 the frequency converter directly receives the output of the buffer) into second data in the frequency domain and to store the second data into the memory (blocks 122 and 126 in figure 5).

Applicant's Argument: Applicant argues, on page 14, the office action does not cite the specific passages of Schmidl that show an FFT unit that is configured to transform first data that is stored in input buffer 122 into second data in the frequency domain and to store the second data into the memory 122.

Examiner's Response: Examiner asserts that Schmidl discloses (see column 16, lines 17-18) that the storage means 122 exchanges data with computing means 124. Other details are shown in Fig. 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Busching et al. (hereafter, referred as Busching) (US 5,778,073), in view of Schmidl et al. (hereafter, referred as Schmidl) (US 5,732,113).

As to claim 1, Busching discloses a receiver apparatus (see Fig. 5), wherein means are provided at the receiver for detection of the preamble within the received information signal. Busching discloses a timing acquisition section that is configured to output a timing signal in response to detection of an end point of the first long preamble (see Fig. 5, block 44). Busching discloses that such means (preamble detection means) initiates (i.e. interpreted as having at least one control signal), as a function of a defined section of the preamble (i.e. end of the preamble, (see column 6, line 19-20)), calculation of the filter coefficients for the frequency domain equalizer filter (see column 11, lines 41-44) in a higher-level computation unit to initialize decryption of the information signal by activating a clock synchronization device (see column 3, lines 27-36). Busching further discloses that the pulse response and the coefficient set for the equalizer filter 51 are calculated with the aid of an FFT (see column 11, lines 40-44). Therefore inherently FFT and equalizer's operation have been controlled by

control signals based one the detection of the preamble in the input signal. Busching does not expressly disclose that the equalizer synchronizes the output of the signal converter in with a clock frequency of the fast Fourier transform processor, and outputs a synchronized second long preamble and second data. However it would have been obvious to one of ordinary skill in the art at the time of invention to synchronize the output of the signal converter with a clock frequency of the FFT to synchronously process the data and preamble and therefore prevent having overflows of data. Busching discloses all the subject matters claimed in claim 1, except that the signal converter is configured to store the first long preamble in response to the first control signal, transform the first long preamble by a fast Fourier transform into a second long preamble, store the second long preamble, transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, output the second long preamble, store the second data, and to output the second data. Schmidl discloses signal converter 120 (see Fig. 5) that is configured to store the first long preamble (i.e. the training signal embedded in the incoming input signal), to transform the first long preamble by a fast Fourier transform into a second long preamble (See block 126), to store the second long preamble (see the arrow from 126 to 122), to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data (see page 16, lines 3-36). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Busching as suggested

by Schmidl to provide fast timing acquisition of the received signal and also enable synchronization to a burst signal for proper reception of the burst data frame (see column 16, lines 15-17).

3. Claim 2-4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busching and Schmidl, in view of Chen et al. (hereafter, referred as Chen) (2003/0050945).

As to claim 2, Schmidl further shows (see Fig. 5) a Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble (i.e. the training symbol) and first data, the FFT processor comprising: an input buffer that is configured to temporarily store the first data (122 in figure 5); a memory that is configured to store the first long preamble (122 in figure 5, note that the symbol include data and training symbol (i.e. preamble), page 16, lines 3-36); and an FFT unit that is configured to transform the first long preamble in the memory into a second long preamble in a frequency domain and to store the second long preamble back into the memory, to transform the first data that is temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory (blocks 122 and 126 in figure 5). Busching and Schmidl disclose all the subject matters claimed in claim 2 except for a memory bank. However, using memory bank to store a data and/or preamble is well known in the art as evidence by Chen (block 70 in figure 5, page 1, paragraph 0007). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of

Chen into the teaching of Busching and Schmidl to reduce hardware cost (column 1, paragraph 0007).

As to claim 3, Chen further discloses that the memory bank includes first, second, third and fourth memories (See Fig. 4, blocks 71A-71D).

As to claim 4, Busching, Schmidl, and Chen do not expressly disclose that the input buffer has a single port and stores N/2-samples of the symbol that is input. However, it would have been a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to use a single port buffer to reduce the cost of the system. Also it would have been obvious to one of ordinary skill in the art at the time of invention to save any number of samples in the memories to meet the system design requirements.

As to claim 6, Schmidl and Chen further disclose the memory bank (block 122 in figure 5 in Schmidl reference using memory bank 70 in Chen reference) is configured to receive the first preamble (signal first coming into the memory/storage from the input signal) and second long preambles (signal coming out of the DFT/FFT and into the memory/storage) and the first data (signal first coming into the storage buffer from the input signal) and second data (signal coming out of the FFT and into the memory) and to output the first and second long preambles and the first and second data so that the memory bank performs an input function and an output function.

As to claim 7, Busching, Schmidl, and Chen do not expressly disclose that each of the first, second, third and fourth memories stores N/2-samples of the symbol. However, saving a certain number of samples of the symbol in each

memory is a matter and design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to save any number of samples in the memories to meet the design requirements.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Busching, Schmidl, and Chen, further in view of He et al. (hereafter, referred as He) (US 6,098,088).

As to claim 5, Busching, Schmidl, and Chen, disclose all the subject matters claimed in claim 2, except that the frequency converter includes a pipelined radix-2 FFT. He discloses that pipelined radix-2 FFT reduces the processing delay of the frequency conversion and also it has a simpler architecture (see column 1, lines 14-16, column 3, lines 10-12, and column 4, lines 20-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Busching, Schmidl, and Chen as suggested by He, for reasons stated above.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Philips (US 5,550,812), Applicant's admitted prior art (background of invention), and Busching, further in view of Schmidl.

As to claim 13, Philips discloses an OFDM receiver (see column 1, lines 30-50) comprising: a quadrature detector that is configured to receive an OFDM signal having a symbol, to convert the OFDM signal into a baseband OFDM signal, to generate a real component of the OFDM signal and an imaginary component of the OFDM signal, and to output the real component of the OFDM signal and the imaginary component of the OFDM signal (See column 1, lines

40-44); an A/D converter that is configured to convert the real and imaginary components of the OFDM signal, respectively, into digital real and imaginary components of a digital OFDM signal, and to output the digital real and imaginary components of the digital OFDM signal (see column 1, lines 44-45); a Fast Fourier Transform processor that is configured to transform the digital OFDM signal by a fast Fourier transform (see column 1, lines 45-46); and a demodulator that is configured to receive the transformed real and imaginary components of the transformed OFDM signal to demodulate the transformed real and imaginary components of the transformed OFDM signal (see column 1, line 46-47). Philips is silent in disclosing that the OFDM signal has a first long preamble. Applicant in the background of invention discloses that OFDM transmitting system transmits a short preamble and a long preamble in the first half of a packet for the purpose of synchronization of a signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips as suggested in the background of invention, for the reason stated above. Phillips and background of invention disclose all the subject matters claimed in claim 13, except that the fast Fourier transform processor comprises: a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the first long preamble; a controller that is configured to output a first control signal and a second control signal in response to the timing signal; a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble,

store the second long preamble, transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, store the second data, and to output the second data; and a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data. Busching discloses a receiver apparatus (see Fig. 5), wherein means are provided at the receiver for detection of the preamble within the received information signal. Busching discloses a timing acquisition section that is configured to output a timing signal in response to detection of an end point of the first long preamble (see Fig. 5, block 44). Busching discloses that such means initiates (i.e. interpreted as having at least one control signal), as a function of a defined section of the preamble (i.e. end of the preamble, (see column 6, line 19-20)), calculation of the filter coefficients for the frequency domain equalizer filter (see column 11, lines 41-44) in a higher-level computation unit to initialize decryption of the information signal by activating a clock synchronization device (see column 3, lines 27-36). Busching further discloses that the pulse response and the coefficient set for the equalizer filter 51 are calculated with the aid of an FFT (see column 11, lines 40-44). Therefore inherently FFT and equalizer's operation have been controlled by control signals based one the detection of the preamble in the input signal. Busching does not expressly disclose that the

equalizer synchronizes the output of the signal converter in with a clock frequency of the fast Fourier transform processor, and to outputs a synchronized second long preamble and second data. However it would have been obvious to one of ordinary skill in the art at the time of invention to synchronize the output of the signal converter with a clock frequency of the FFT to synchronously process the data and preamble and therefore prevent having overflows of data. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips and Applicant's background of invention, and suggested by Busching to synchronize the receiver. Philips, Applicant's background of invention, and Busching disclose all the subject matters claimed in claim 13, except that the signal converter is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data. Schmidl discloses signal converter 120 (see Fig. 5) that is configured to store the first long preamble (i.e. the training signal embedded in the incoming input signal), to transform the first long preamble by a fast Fourier transform into a second long preamble (See block 126), to store the second long preamble (see the arrow from 126 to 122), to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the

second data (see page 16, lines 3-36). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Philips, Applicant's background of invention, and Busching as suggested by Schmidl to provide fast timing acquisition of the received signal and also enable synchronization to a burst signal for proper reception of the burst data frame (see column 16, lines 15-17).

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Philips, Applicant's admitted prior art (background of invention), Busching, and Schmidl, further in view of Chen.

As to claim 14, Schmidl shows (see Fig. 5) a Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble (i.e. the training symbol) and first data, the FFT processor comprising: an input buffer that is configured to temporarily store the first data (122 in figure 5); a memory that is configured to store the first long preamble (122 in figure 5, note that the symbol include data and training symbol (i.e. preamble), page 16, lines 3-36); and an FFT unit that is configured to transform the first long preamble in the memory into a second long preamble in a frequency domain and to store the second long preamble back into the memory, to transform the first data that is temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory (blocks 122 and 126 in figure 5). Philips, Applicant's background of invention, Busching, and Schmidl disclose all the subject matters claimed in claim 14 except for a memory bank. However,

using memory bank to store a signal data and preamble is well known in the art as evidence by Chen (block 70 in figure 5, page 1, paragraph 0007). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Chen into the teaching of Busching and Schmidl to reduce hardware cost (column 1, paragraph 0007).

As to claim 15, Schmidl and Chen further disclose the memory bank (block 122 in figure 5 in Schmidl reference using memory bank 70 in Chen reference) is configured to receive the first preamble (signal first coming into the memory/storage from the input signal) and second long preambles (signal coming out of the DFT/FFT and into the memory/storage) and the first data (signal first coming into the storage buffer from the input signal) and second data (signal coming out of the FFT and into the memory) and to output the first and second long preambles and the first and second data so that the memory bank performs an input function and an output function.

As to claim 16, Chen further discloses that the memory bank includes first, second, third and fourth memories (See Fig. 4, blocks 71A-71D). Philips, Applicant's admitted prior art, Busching, Schmidl, and Chen do not expressly disclose that each of the first, second, third and fourth memories stores N/2-samples of the symbol. However, saving a certain number of samples of the symbol in each memory is a matter and design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to save any number of samples in the memories to meet the system design requirements.

As to claim 17, Philips, Applicant's admitted prior art, Busching, Schmidl, and Chen do not expressly disclose that the input buffer has a single port and stores N/2-samples of the symbol that is input. However, it would have been a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to use a single port buffer to reduce the cost of the system. Also it would have been obvious to one of ordinary skill in the art at the time of invention to save any number of samples in the memories to meet the system design requirements.

7. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidl, in view of Chen.

As to claim 18, Schmidl shows (see Fig. 5) a Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble (i.e. the training symbol) and first data, the FFT processor comprising: an input buffer that is configured to temporarily store the first data (122 in figure 5); a memory that is configured to store the first long preamble (122 in figure 5, note that the symbol include data and training symbol (i.e. preamble), page 16, lines 3-36); and an FFT unit that is configured to transform the first long preamble in the memory into a second long preamble in a frequency domain and to store the second long preamble back into the memory, to transform the first data that is temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory (blocks 122 and 126 in figure 5). Busching and Schmidl disclose all the subject matters claimed in claim 18

except for a memory bank. However, using memory bank to store a signal data and preamble is well known in the art as evidence by Chen (block 70 in figure 5, page 1, paragraph 0007). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Chen into the teaching of Schmidl to reduce hardware cost (column 1, paragraph 0007).

As to claim 19, Schmidl and Chen further disclose the memory bank (block 122 in figure 5 in Schmidl reference using memory bank 70 in Chen reference) is configured to receive the first preamble (signal first coming into the memory/storage from the input signal) and second long preambles (signal coming out of the DFT/FFT and into the memory/storage) and the first data (signal first coming into the storage buffer from the input signal) and second data (signal coming out of the FFT and into the memory) and to output the first and second long preambles and the first and second data so that the memory bank performs an input function and an output function.

Allowable Subject Matter

8. Claims 8-12 allowed. The following is a statement of reasons for the indication of allowable subject matter: a comprehensive search of prior art of record failed to disclose, either alone or in combination, a method of transforming an OFDM signal by a fast Fourier transform, the OFDM signal having a symbol, the symbol including a first long preamble, a second long preamble and first data, the method comprising: (a) storing the first long preamble and the second long

preamble in first, second, third and fourth memories in sequence as the OFDM signal is received; (b) reading the first long preamble and the second long preamble stored in the first, second, third and fourth memories in response to an end point of the second long preamble being detected, transforming the first and second long preambles by a fast Fourier transform, respectively, into a third preamble and a fourth preamble, and storing in sequence the third and fourth long preambles in the first memory and the second memory; (c) transforming second data that is input after first data is buffered, and the first data that is directly input, respectively, into third data when the first and second long preambles are transformed into the third and fourth data, storing the third data in the memories in sequence, and outputting the third data stored in the memories; and (d) finishing the fast Fourier transform method when the symbol is a final symbol, and performing (c) when the symbol is not the final symbol.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leila Malek whose telephone number is 571-272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

L.M.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER